Optimizing the Power-Added Efficiency of a Class B GaAs FET Amplifier

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Abstract

The paper reports on a design routine which optimizes the power-added efficiency of a Class B microwave amplifier stage. Experimental results at 4.4 GHz are reported which support the procedure and show efficiency increases of 15% when low impedance loading at even harmonic frequencies are provided.

Introduction

There are a number of variables which must be considered when designing a GaAs FET amplifier for maximum power-added efficiency. These variables include: conduction angle, drain bias voltage and the load impedance at both the fundamental and harmonic frequencies. Conduction angle is a variable because of the non-abrupt pinch-off associated with GaAs FETs. Predicting and experimentally determining optimum values for these variables is addressed in this paper in which the design and testing of a 4.4 GHz amplifier is reported.

One possible approach to the problem of maximizing power-added efficiency involves idealizing the device characteristics and circuit to the point where a simple analysis is possible. A much more accurate and time-consuming approach would be to use a large-signal simulation program such as SPICE or a more time efficient method such as the harmonic balance simulation technique. An optimization routine which uses a simulation program to test various combinations of the aforementioned variables can then be used to predict the optimum power-added efficiency for a particular device.

The method presented in this paper falls between the above approaches in complexity yet yields insight and fairly accurate solutions. The measured data required consists of device I-V data and one large-signal gain measurement at the microwave frequency of interest. The method is based on a simple circuit model from which the power-added efficiencies, resulting from a specific combination of the variables, can be calculated.

Similar to the harmonic balance method this simulation iterates between time domain and frequency domain solutions until agreement is reached.

RF I-V Measurement

RF (≥1MHz) I-V measurements are more accurate and relevant to microwave behavior than DC I-V measurements for three reasons: 1. Trapping effects are included.[1] 2. The instantaneous channel temperature can be held controlled while the measurement is being made. 3. The device dissipation at RF can be made to match the device dissipation at the microwave frequency.

While the device was operating at 11MHz, the instantaneous gate and drain voltages and drain current were measured with probes and an oscilloscope. A schematic of the measurement set-up is shown in Fig. 1.

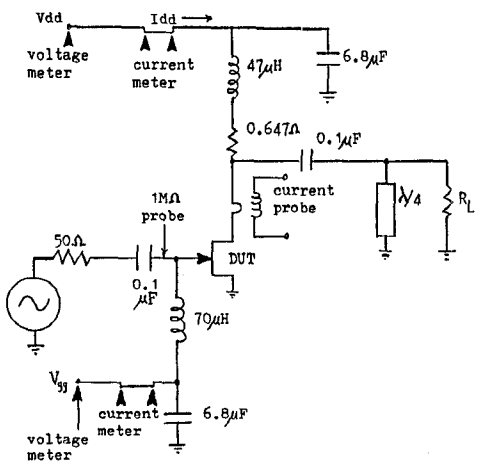

Fig. 1. RF I-V curve tracer.

The data points were gathered at 1V increments of V_{GS} and the associated V_{DS} and I_{DS} were

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recorded. Next the drain voltage bias was increased by 1V and another set of data points were measured in the same way. The load resistance was adjusted as V_{DD} was increased to keep the power dissipated in the device constant. With this technique, device dissipation at 11MHz could be adjusted to match device dissipation at the microwave frequency of interest. Therefore the channel temperature was made to equal the channel temperature at the microwave operation being modelled. The rate of 11MHz insured that trapping and thermal time constants were not affecting the measurement.

An example of the measured current waveforms for increasingly larger V_{DD} are shown in Fig. 2.

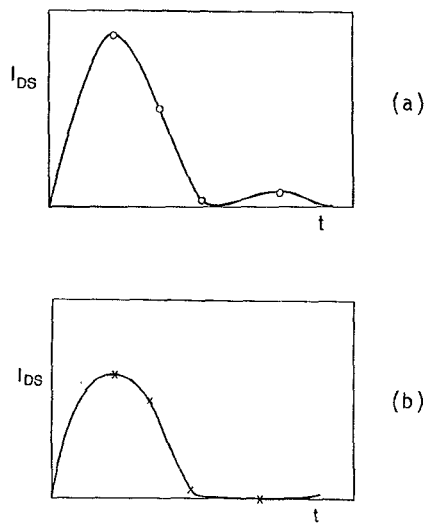

Fig. 2. Typical measured drain currents.

In waveform 2(a), the peak of the current is occurring below the knee of the I-V curves thus distorting the waveform. In waveform 2(b) drain-to-gate breakdown current is evident. Figure 3 shows how the data points result in the family of RF output characteristics.

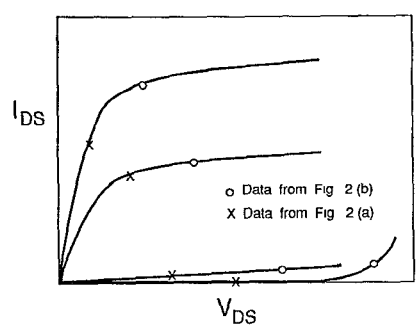

Fig. 3. RF output characteristics generated from data of Fig. 2.

Optimization/Simulation Program

Figure 4 shows the circuit model used for the simulation routine. The model includes the effects of the gate and drain bias voltages. The drain to source capacitance, C_{DS}, which has been separated from the "intrinsic FET." A complex load is assumed but the load inductance is adjusted to cancel the reactance of C_{DS} at high efficiency operation. Therefore the "intrinsic FET" drives a purely resistive load in the model.

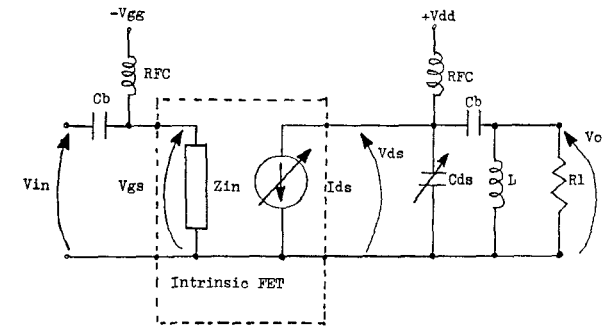

Fig. 4. Circuit model used in optimization program

The program computes the highest power-added efficiency possible for conduction angles between class A and B. The optimum drain bias voltage and load resistance for each conduction angle is also predicted.

The program works as follows. For a given conduction angle, a sinusoidal gate voltage waveform is calculated on the basis of the pinch-off voltage of that device. With a selection of drain bias voltage, V_{DD}, and load resistance, R_L, together with an initial drain to source voltage amplitude, V_{DS}, a corresponding drain current waveform can be computed from the I-V data. Rather than fitting the I-V data to an equation, a look-up table of the measured I-V data and an interpolation routine gives I_{DS} as a function of V_{GS} and V_{DS}. A discrete Fourier transform is performed on the drain current waveform to calculate the fundamental component. The DC component of the current is also calculated. The fundamental component of the current is multiplied by the load resistance to calculate the magnitude of the new and more accurate time domain solution of V_{DS}. This loop continues until a solution ceases to change appreciably.

Because V_{DD} was selected and the DC drain current was computed, the input DC power is known. The AC drain voltage and current were found and assumed to be in phase so the output power can also be determined. Thus drain efficiency can be computed. The amount of power delivered to the gate is computed on the basis of the magnitude of the driving voltage. This input

power is correlated to the microwave gain data taken under known operating conditions. With the input and output microwave power calculated along with the DC power, the power-added efficiency is determined.

A search routine tests various combinations of V_{DD} and R_L until the optimum combination is found which maximizes the power-added efficiency. Next another conduction angle is chosen and the above process repeats itself.

Evaluation of Power and Efficiency Measurements

The "intrinsic FET" model, shown in Figure 4 uses an ideal representation of the matching circuit on the output of the FET. The actual loading circuit used in the experiment, shown in Figure 6, utilizes a short-circuited quarter-wave stub to obtain harmonic cancellation, followed by a matching circuit that provides optimum efficiency at the fundamental frequency. Intuitively it is straightforward to see that reducing the harmonic output power improves the efficiency of an amplifier. Specifically, suppressing harmonic voltage while retaining a half sine wave pulsating current minimizes device dissipation. To see this effect first consider the case where the fundamental signal and the 2nd harmonic are terminated in a 50Ω load.

The well-known upper limit Class "B" for collector efficiency, η, for this case is 78.5% ($\pi/4$). The efficiency is given by

$$\eta = \frac{P_{DC}-P_{DISS}}{P_{DC}} \% \ , \qquad (1)$$

where we assume $V_{sat} = 0$ and a sharp cutoff in the characteristics of the FET, see Fig. 5. Now we can write,

$$\frac{V_1}{I_1} = \frac{V_2}{I_2} \qquad (2)$$

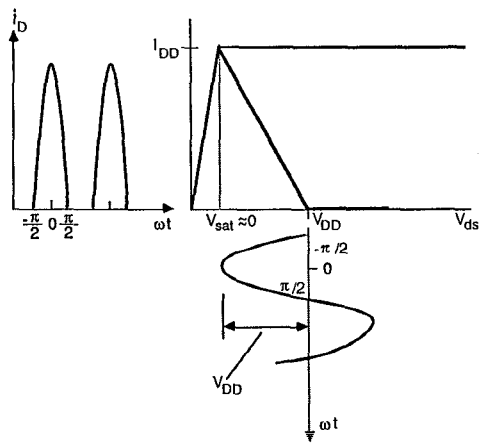

Fig. 5. Ideal RF output characteristics

To determine V_2 equate the peak value of the halfwave sinusoid to the saturation current, I_{DD}, and V_1 to V_{DD}, see Fig. 5. Then using the Fourier coefficients of a halfwave sinusoid,

$$I_{DC} = \frac{I_{DD}}{\pi} \ , \quad I_1 = \frac{I_{DD}}{2} \ , \quad I_2 = \frac{2I_{DD}}{3\pi} \qquad (3)$$

We can write V_2 as:

$$V_2 = \frac{4V_{DD}}{3\pi} \qquad (4)$$

So the power dissipated in the device due to the presence of the second harmonic voltage is

$$P_{2DISS} = \frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} (I_{DD}\cos\omega t)\left(\frac{4V_{DD}}{3\pi}\sin 2\omega t\right)d\omega t = \frac{4V_{DD}I_{DD}}{9\pi^2} \qquad (5)$$

This term, substituted into P_{DISS} in Eq. 1, reduces the collector efficiency by 14.1%. A reduction in the harmonic load reduces the harmonic voltage while the current waveform retains its nonlinearity. In the experiment performed we reduced the harmonic load from 50Ω to 5Ω, ideally this represents an increase in efficiency from 64.4% to 77.1%, a 13.3% change in collector efficiency.

The power gain and efficiency measurements were obtained with the set-up shown in Fig. 6.

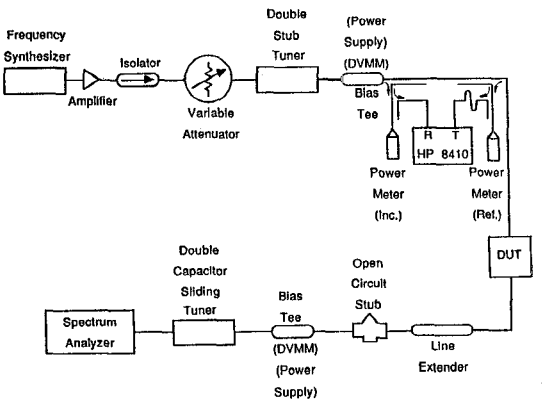

Fig. 6. Microwave efficiency experiment.

This set-up provides the means for measuring input power, input reflection coefficient and the output power. With these measurements, along with the bias levels, we can determine the power gain, conduction angle and the power-added efficiency. The harmonic loading consists of a coaxial line extender and a tee (type SMA). Due to obvious DC biasing problems in using a shorted quarter-wave stub, an open SMA barrel was connected to the tee

and the nonideal nature of the tee provided a frequency response that resembles a shorted quarter-wave stub. This quarter-wave stub provides a second harmonic load of 5Ω, and the fundamental load is completely determined by the double stub tuner. The effective short at the harmonic frequencies provides a direct path for the harmonic currents to the source, while also suppressing the harmonic voltages induced by the transistor.

Results and Conclusions

The results of the simulation and measurements are shown in Figs. 7, 8 and Table 1. The plots show the amount of agreement between the simulated versus measured results.

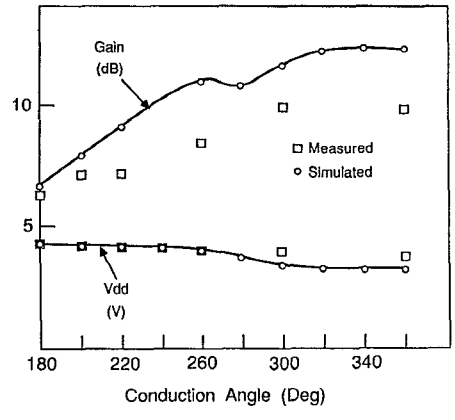

Fig. 7. Gain and V_{DD} versus conduction angle.

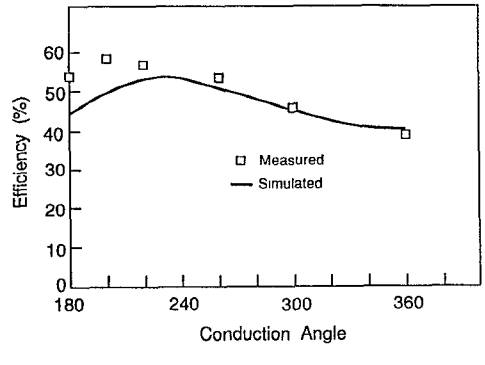

Fig. 8. Power-added efficiency versus conduction angle.

Note in Figure 8 the power-added efficiency peaks at a conduction angle of 200°, due to the non-abrupt pinch-off characteristics of the GaAs FETs. In Table 1, the effect of the second harmonic impedance is shown to and agrees with expected changes in efficiency computed above.

Table 1

Fundamental Load (ohms)	Harmonic Load (ohms)	Power-added Efficiency	Change in Efficiency
42-j20.0	38-j3	46.3%	-
42-j21.5	5.0	61.7%	15.4%
25.0	42+j12.5	31.2%	-
25.0	5.0	45.6%	14.4%

Note: Bias levels were held constant for both harmonic load cases.

The authors would like to add that a monolithic version of the experiment is being processed and is expected to show clearly the effect of harmonic loading on power-added efficiency. This technique, after refinement for better accuracy, holds promise for: 1) evaluating new microwave power devices, 2) gaining insight into the inter-relations of MESFET characteristics which determine efficiency, and 3) aiding in initial designs of power amplifiers.

Acknowledgements

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Reference

1. Smith, M., T. Howard, K. Anderson and A. Pavio, "RF Nonlinear Device Characterization Yield Improved Modelling Accuracy," 1986 MTT-S Digest.